F I G. 1

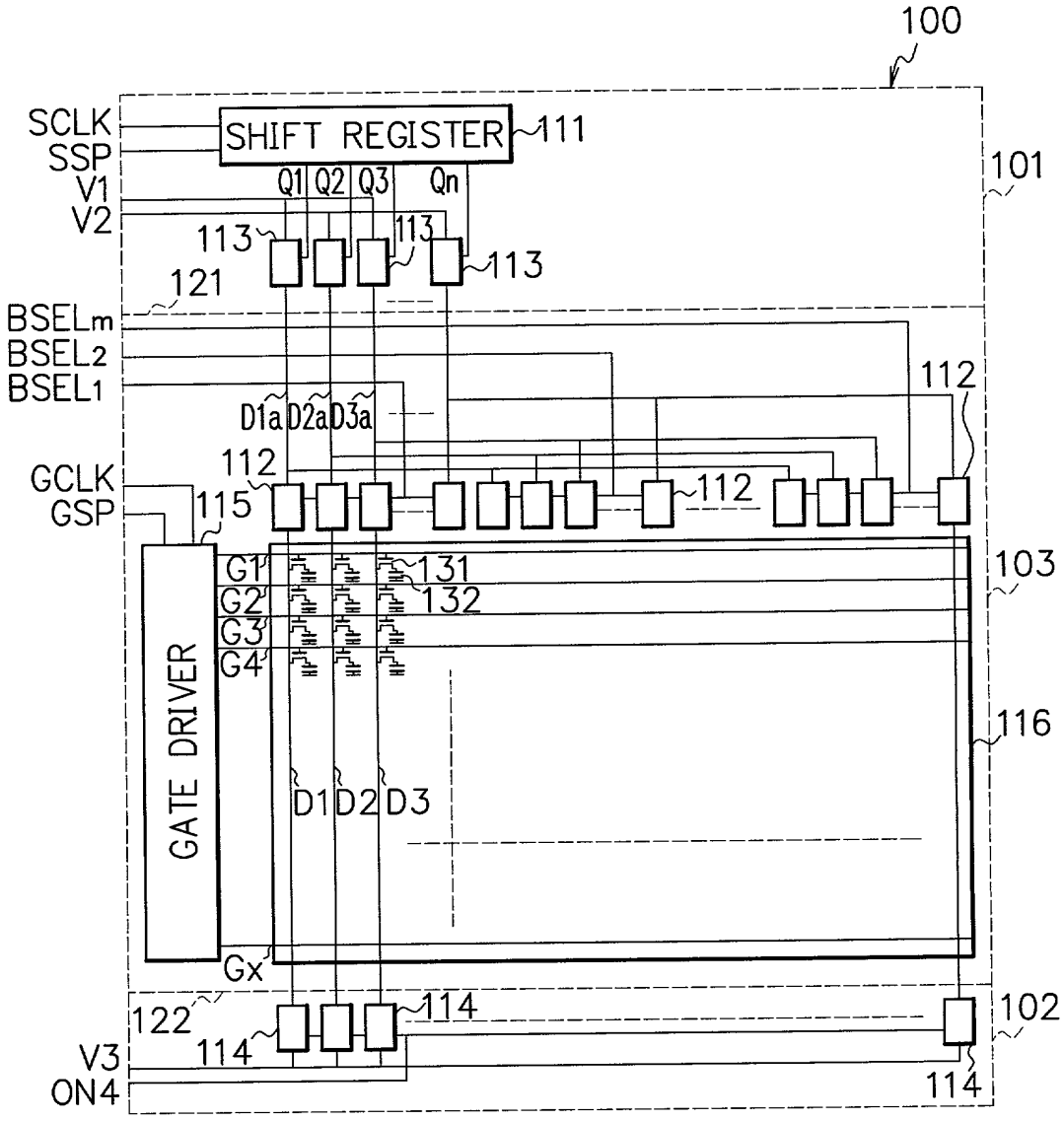

100
SCLK
SSP
V1
V2
SHIFT REGISTER
111
Q1
Q2
Q3
Qn
101
113
121
BSELm
BSEL2
BSEL1
D1a
D2a
D3a
112
GCLK
GSP
115
131
132
G1
G2
G3
G4
103
GATE DRIVER
116
D1
D2
D3
Gx
122
114
V3
ON4
102

FIG. 2

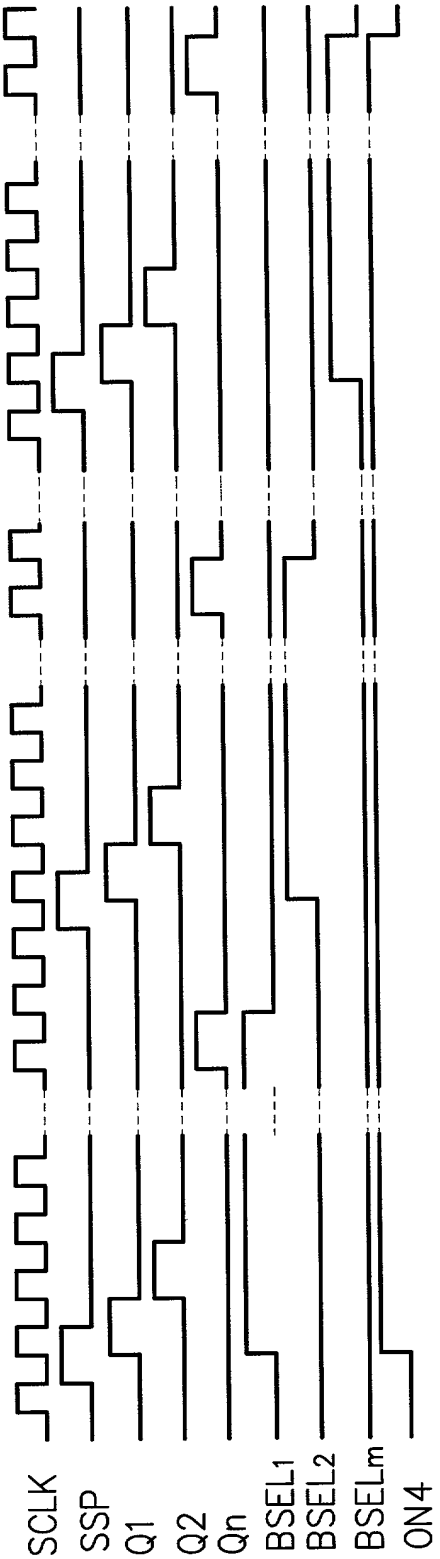


FIG. 3

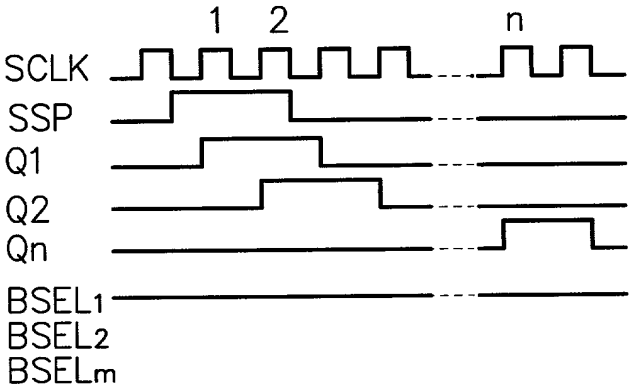
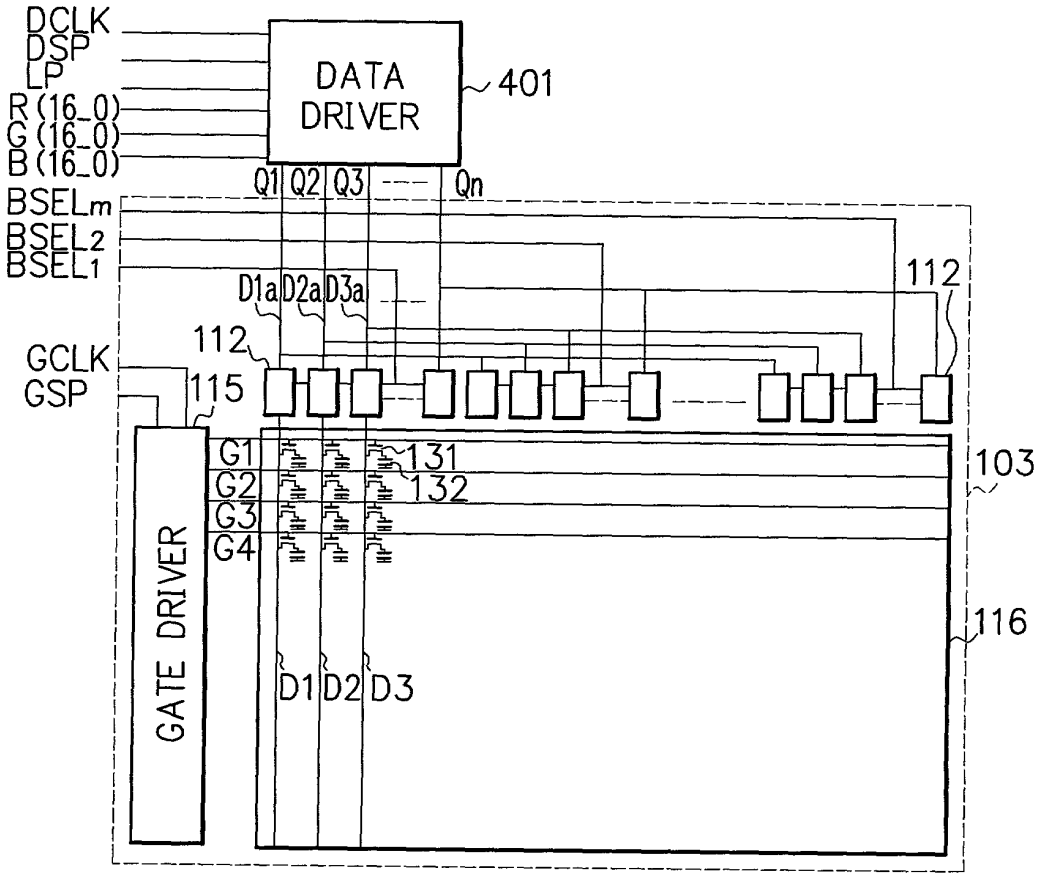
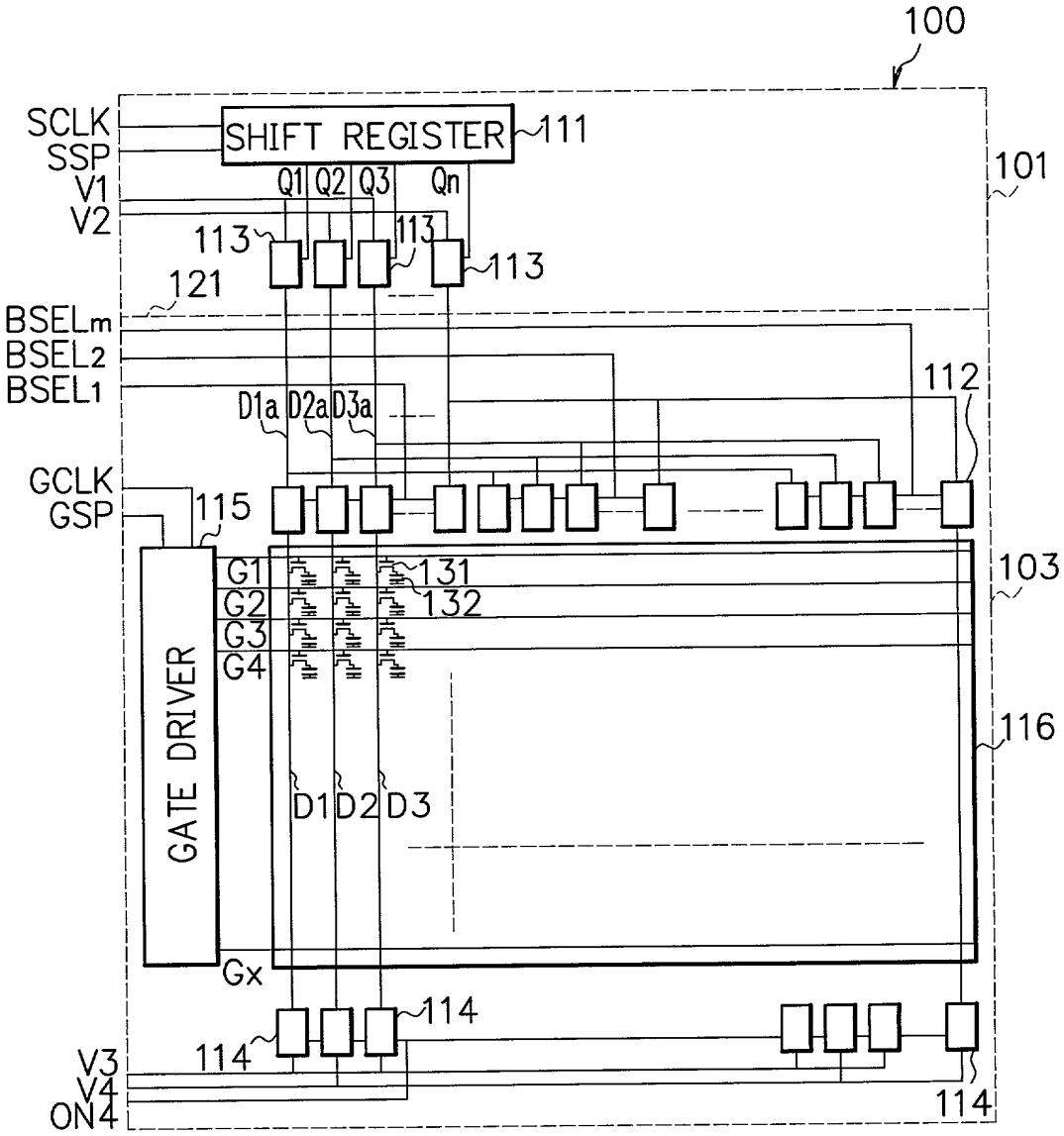


FIG. 4


DCLK
DSP
LP
R(16_0)
G(16_0)
B(16_0)
DATA DRIVER
401
Q1 Q2 Q3 --- Qn
BSELm
BSEL2
BSEL1
D1a D2a D3a
112
112
GCLK
GSP
115
G1
G2
G3
G4
131
132
103
GATE DRIVER
116
D1 D2 D3

F I G. 5


100
SCLK
SSP
V1
V2
SHIFT REGISTER
111
Q1
Q2
Q3
Qn
101
113
113
113
121
BSELm
BSEL2
BSEL1
D1a
D2a
D3a
112
GCLK
GSP
115
G1
G2
G3
G4
131
132
103
GATE DRIVER
116
D1
D2
D3
Gx
114
114
V3
V4
ON4
114

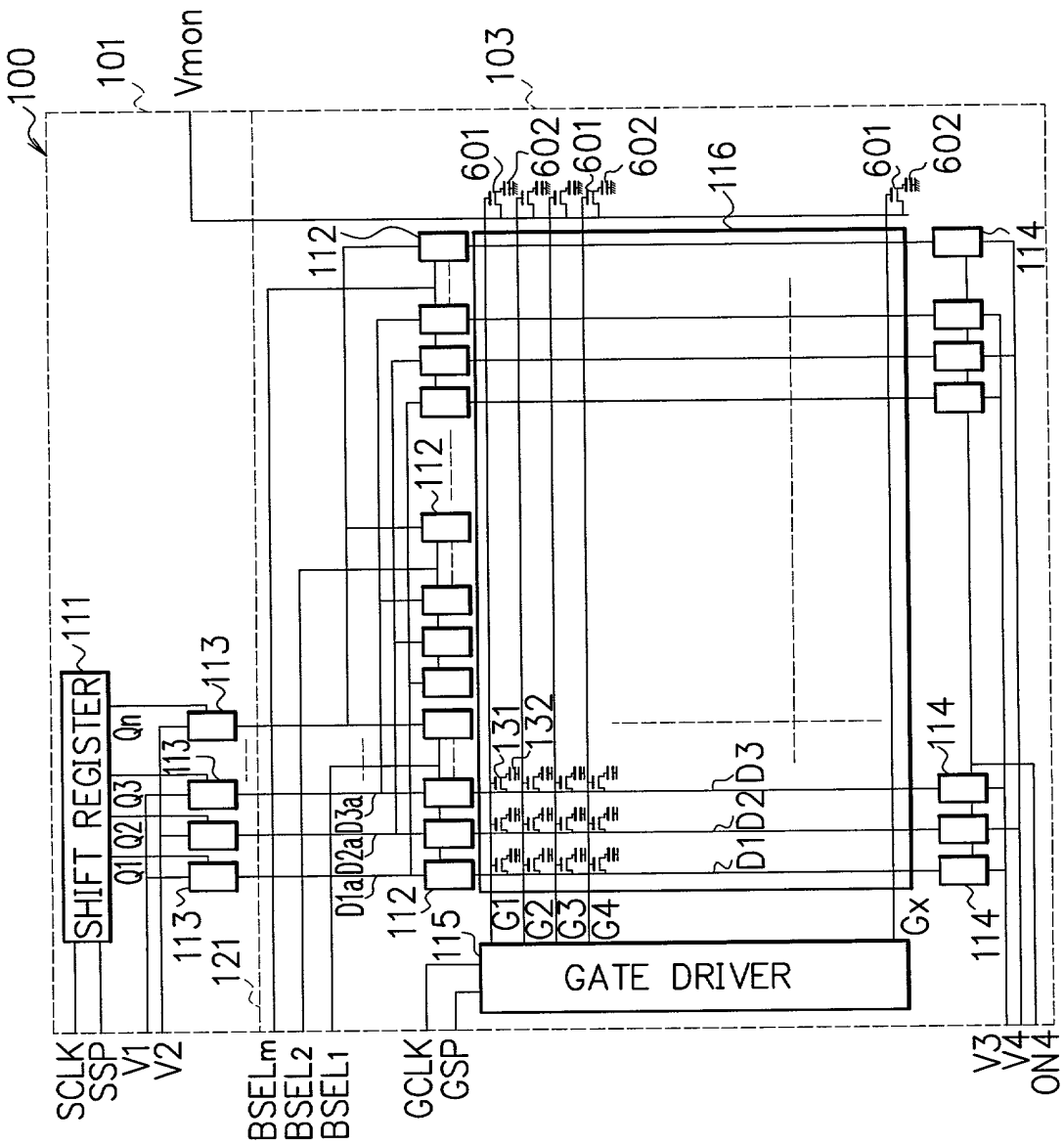

100
101
Vmon
103
601
602
116
112
114
SHIFT REGISTER
111
113
Qn
Q1 Q2 Q3
131
132
D1 D2 D3
D1a D2a D3a
G1 G2 G3 G4
Gx
115
121
GATE DRIVER
SCLK
SSP
V1
V2
BSELm
BSEL2
BSEL1
GCLK
GSP
V3
V4
ON4

FIG. 6

FIG. 7

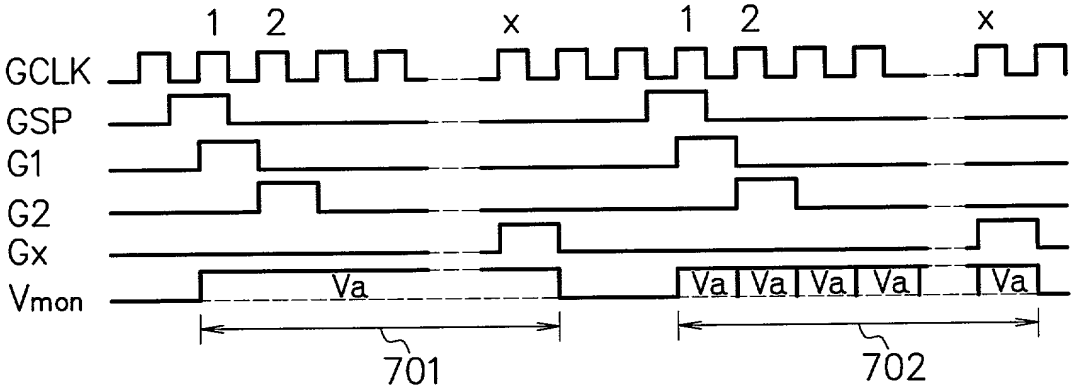

1
2
x
1
2
x
GCLK
GSP
G1
G2
Gx
Vmon
Va
Va
Va
Va
Va
Va
701
702

FIG. 8

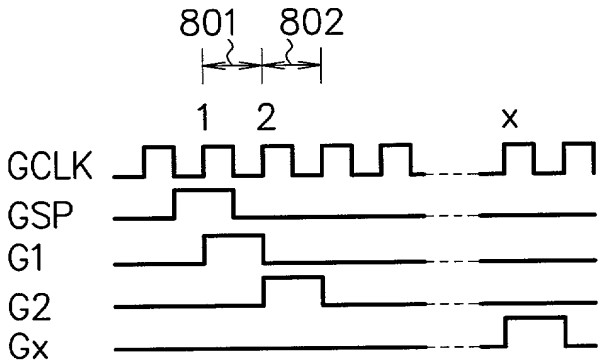

801
802
1
2
x
GCLK
GSP
G1
G2
Gx

FIG. 9

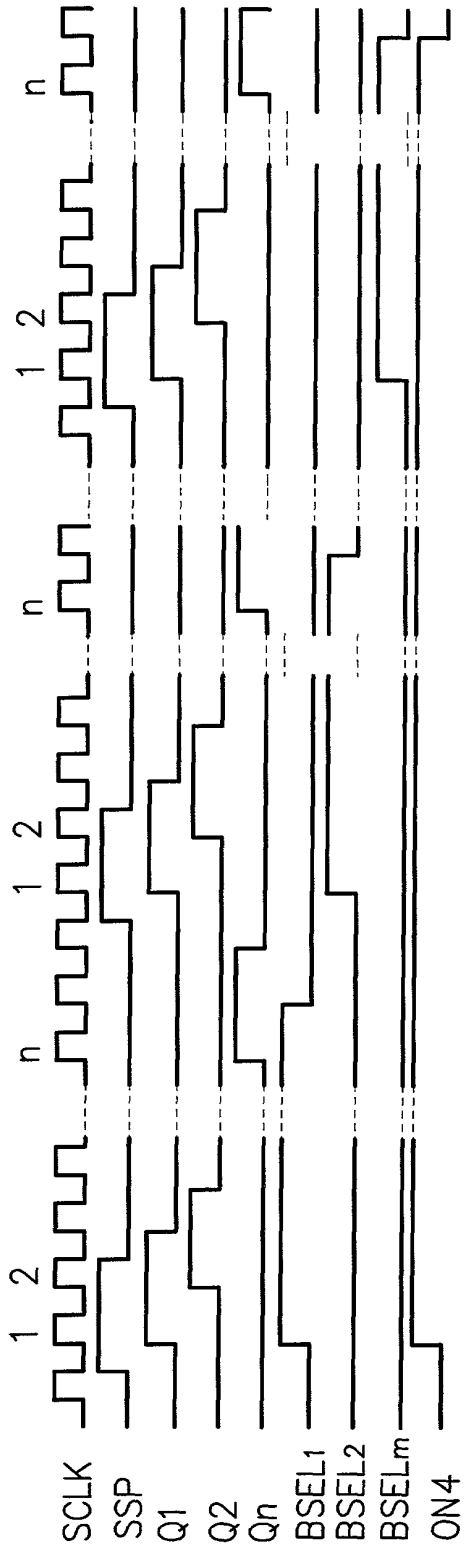
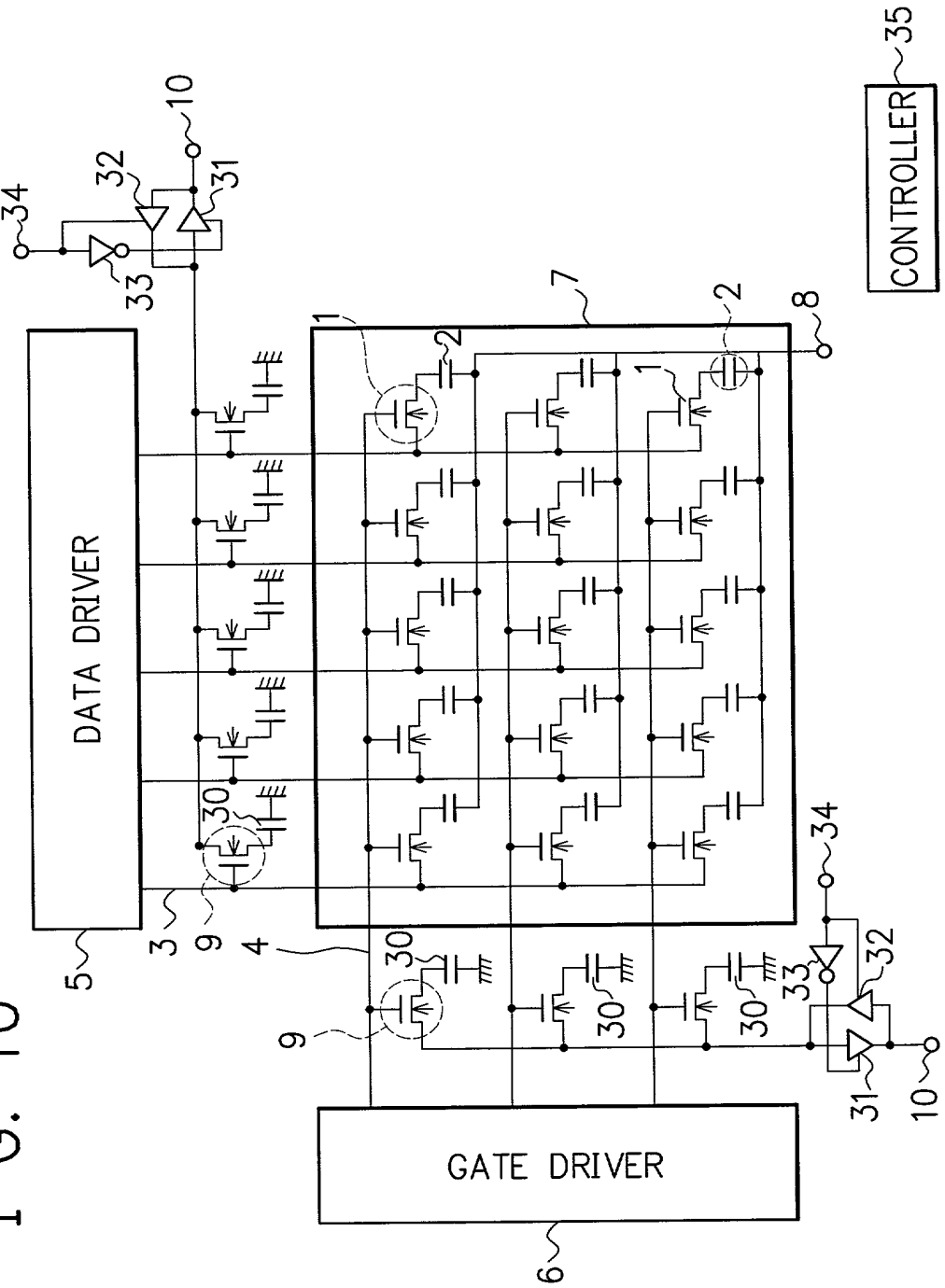


FIG. 10


CONTROLLER
35
DATA DRIVER
GATE DRIVER
1
2
3
4
5
6
7
8
9
10
30
31
32
33
34

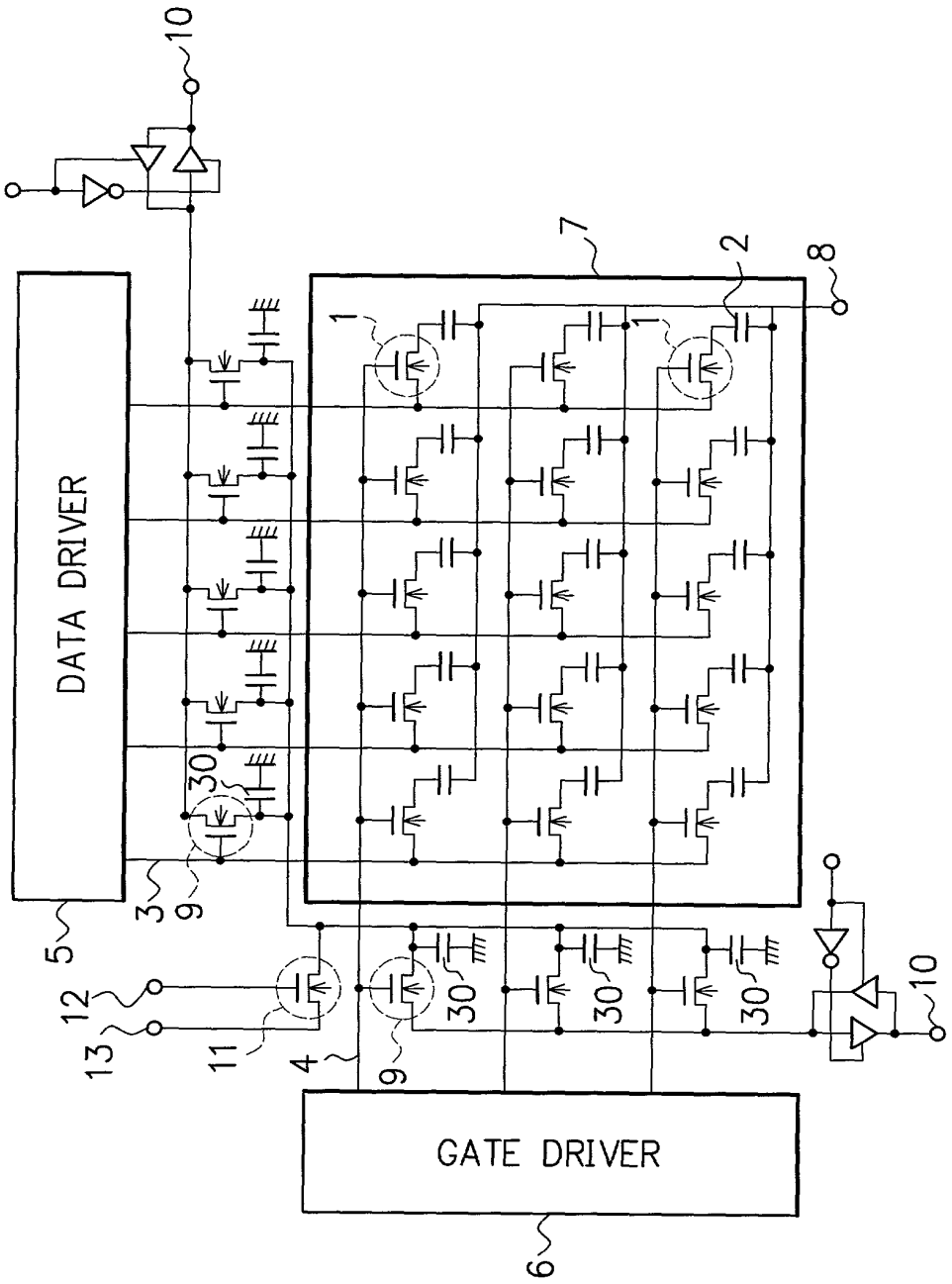


FIG. 11

FIG. 12

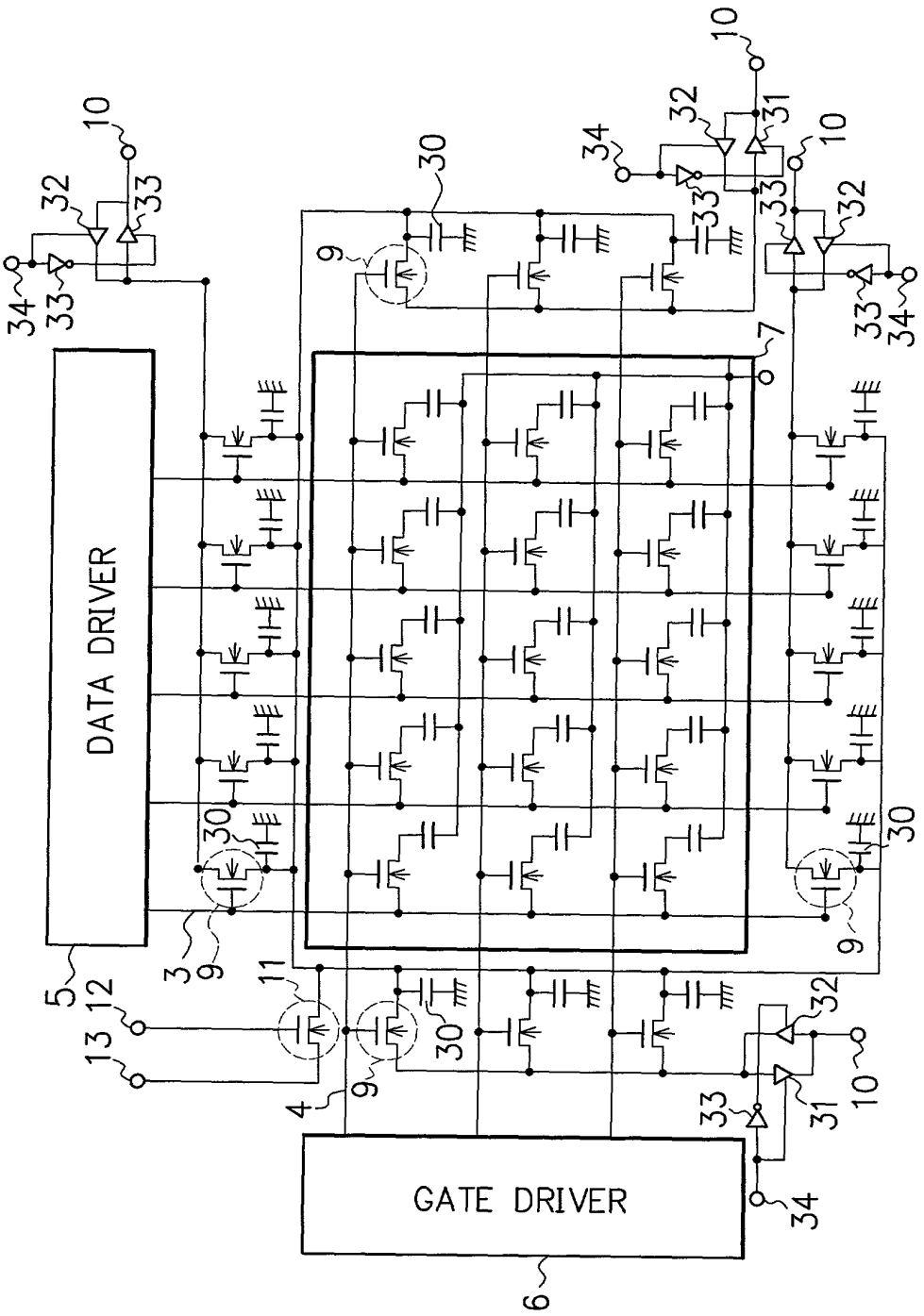


FIG. 13

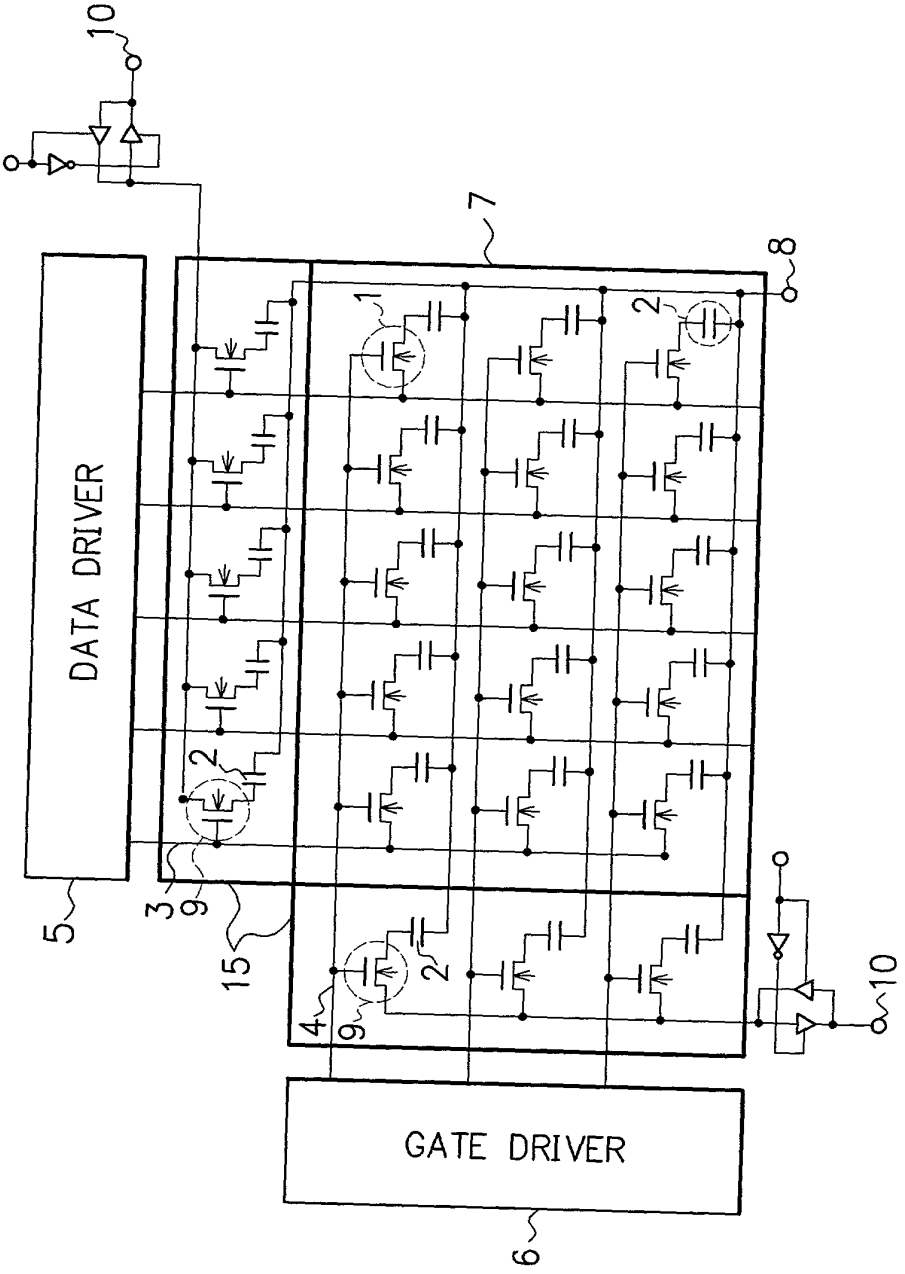
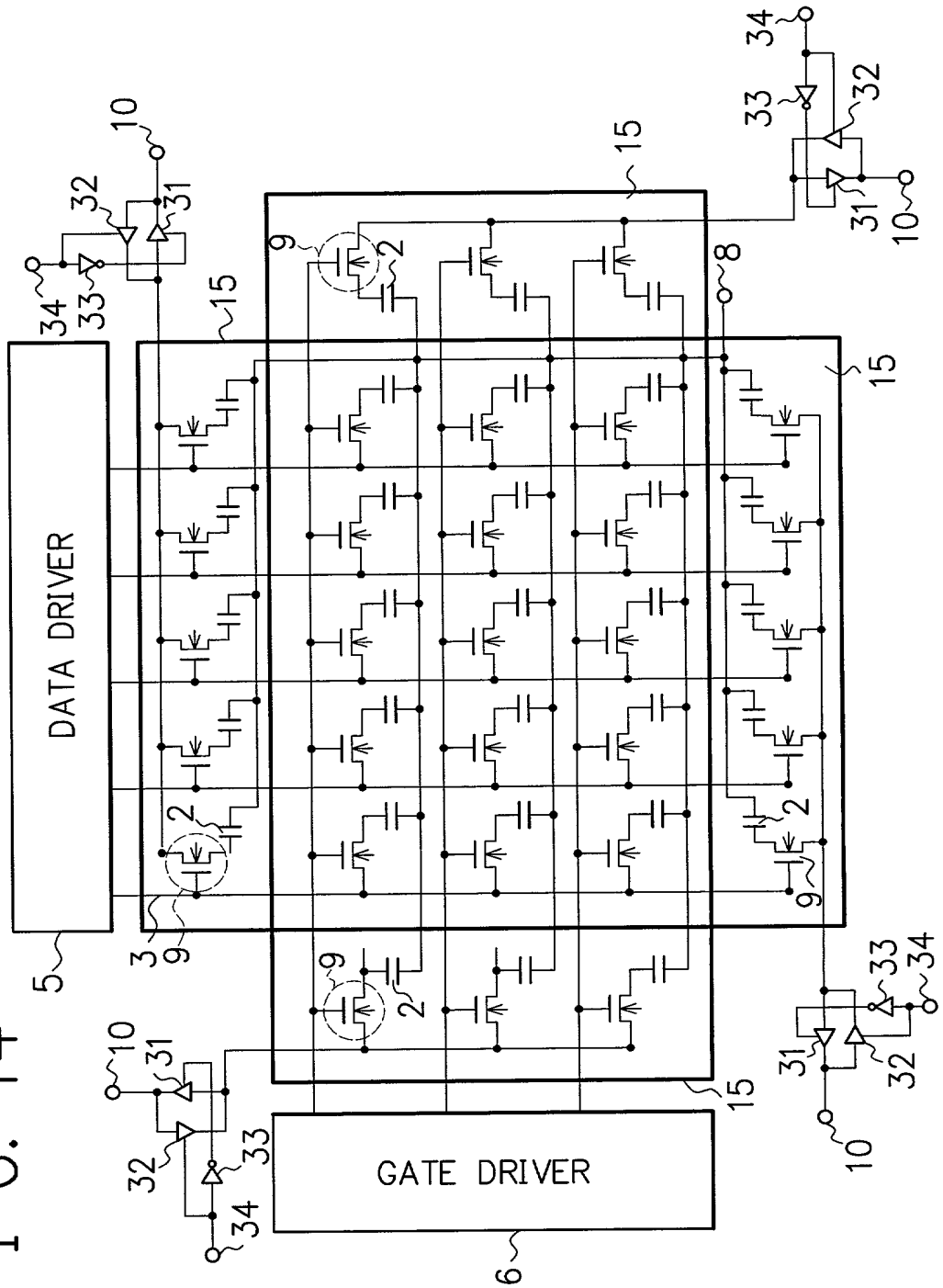


FIG. 14



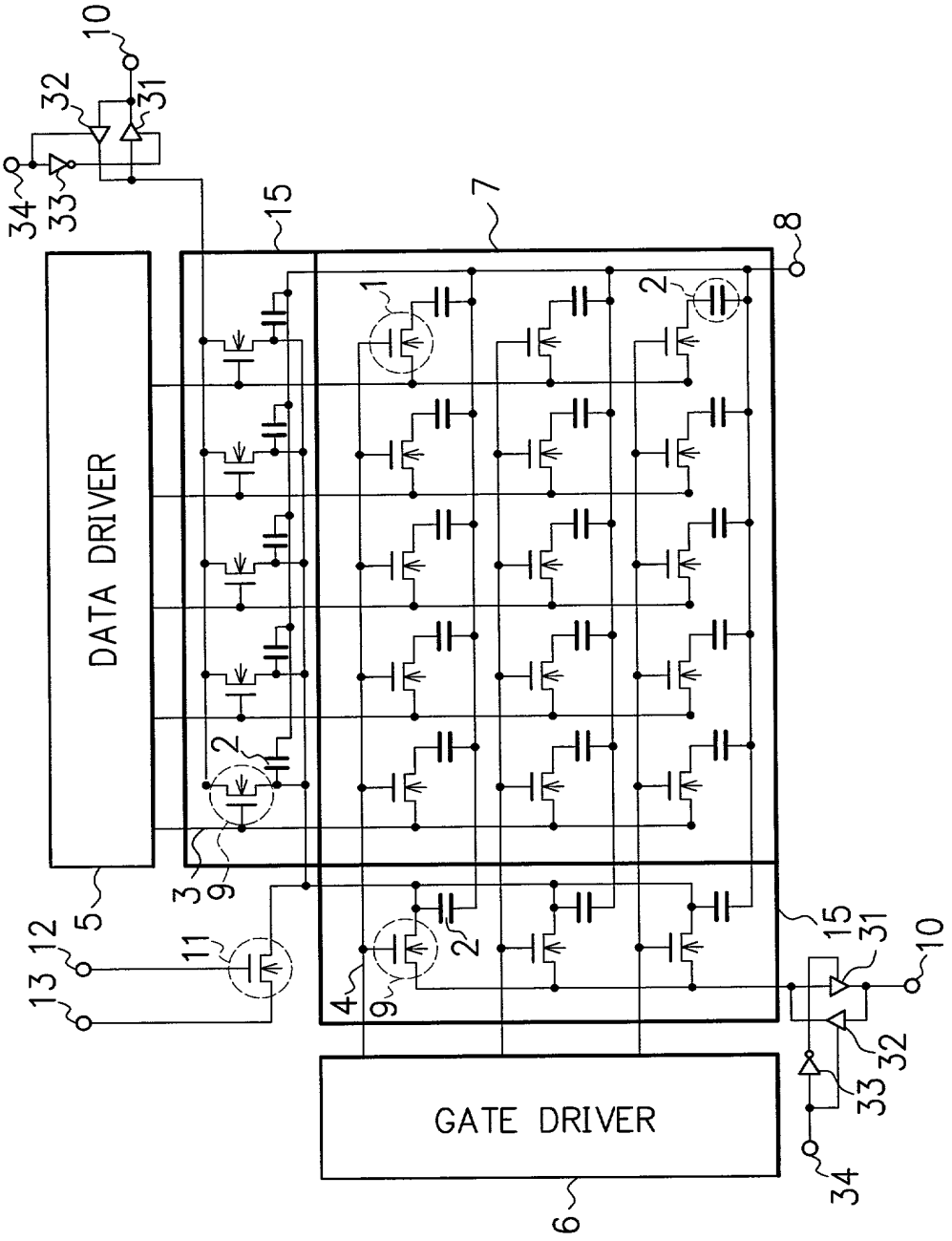


FIG. 15

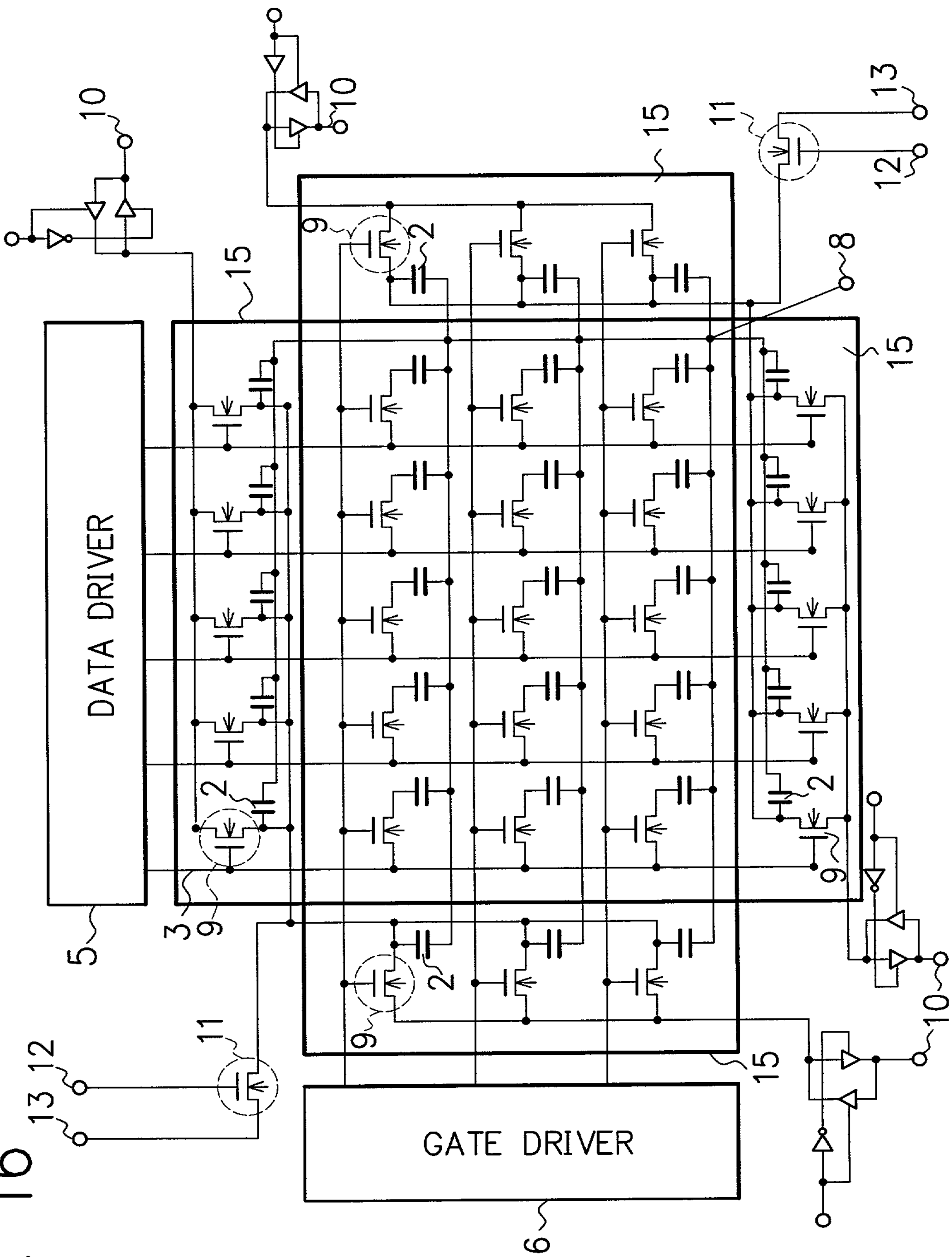


FIG. 16

FIG. 17

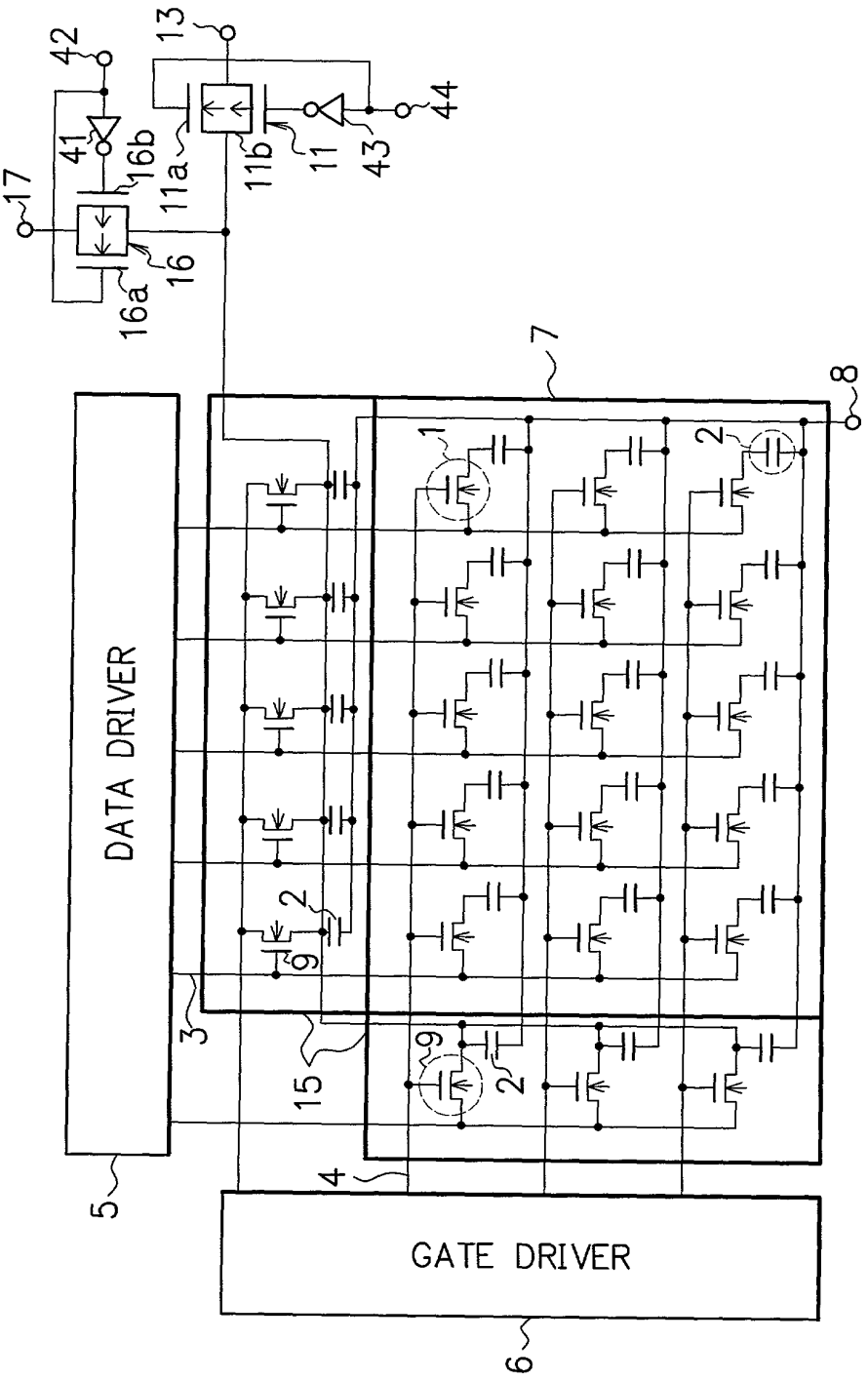

42
13
41
16b
11a
11b
11
43
44
17
16
16a
7
8
1
2
DATA DRIVER
9
3
15
4
5
GATE DRIVER
6

FIG. 18

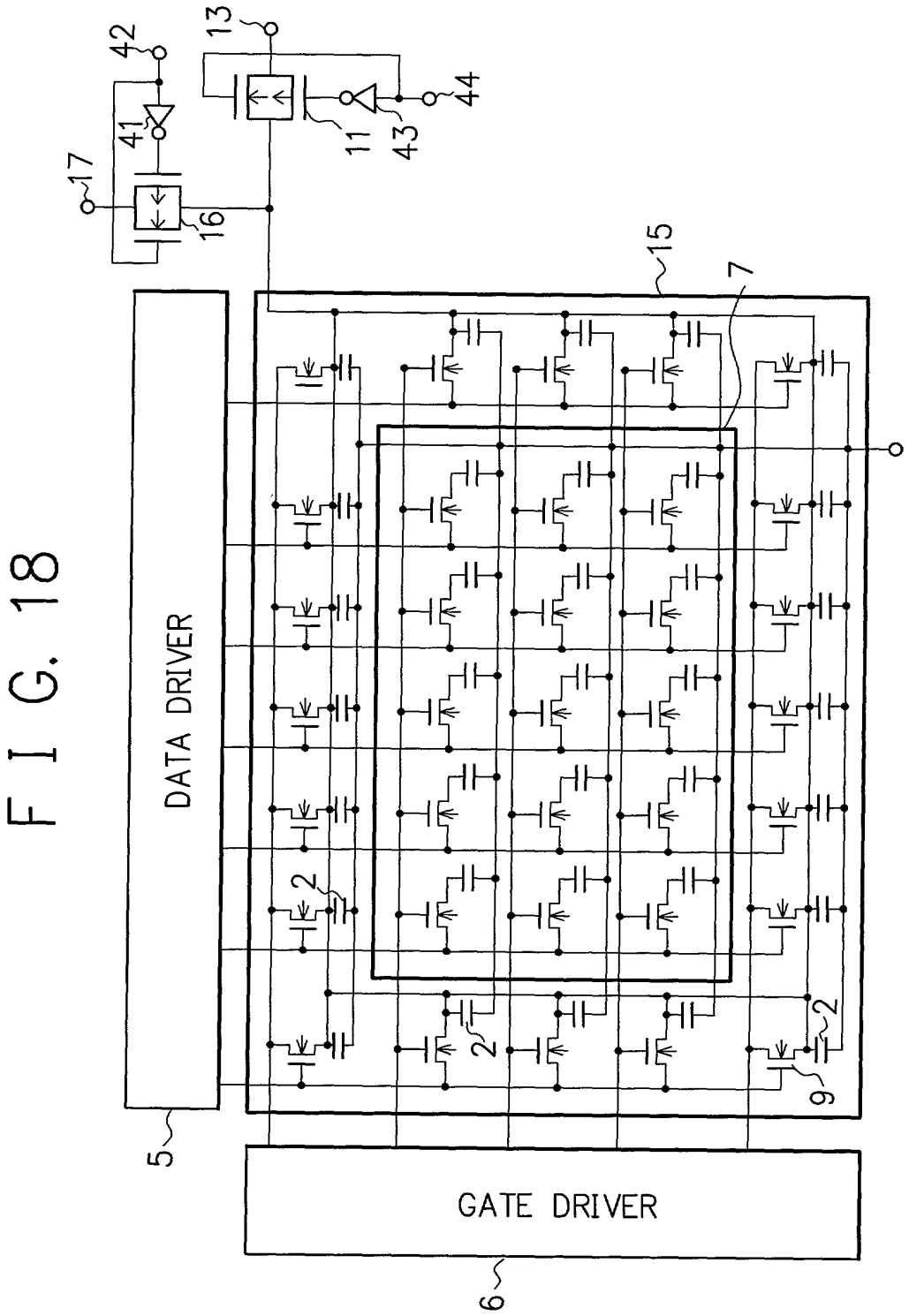


FIG. 19

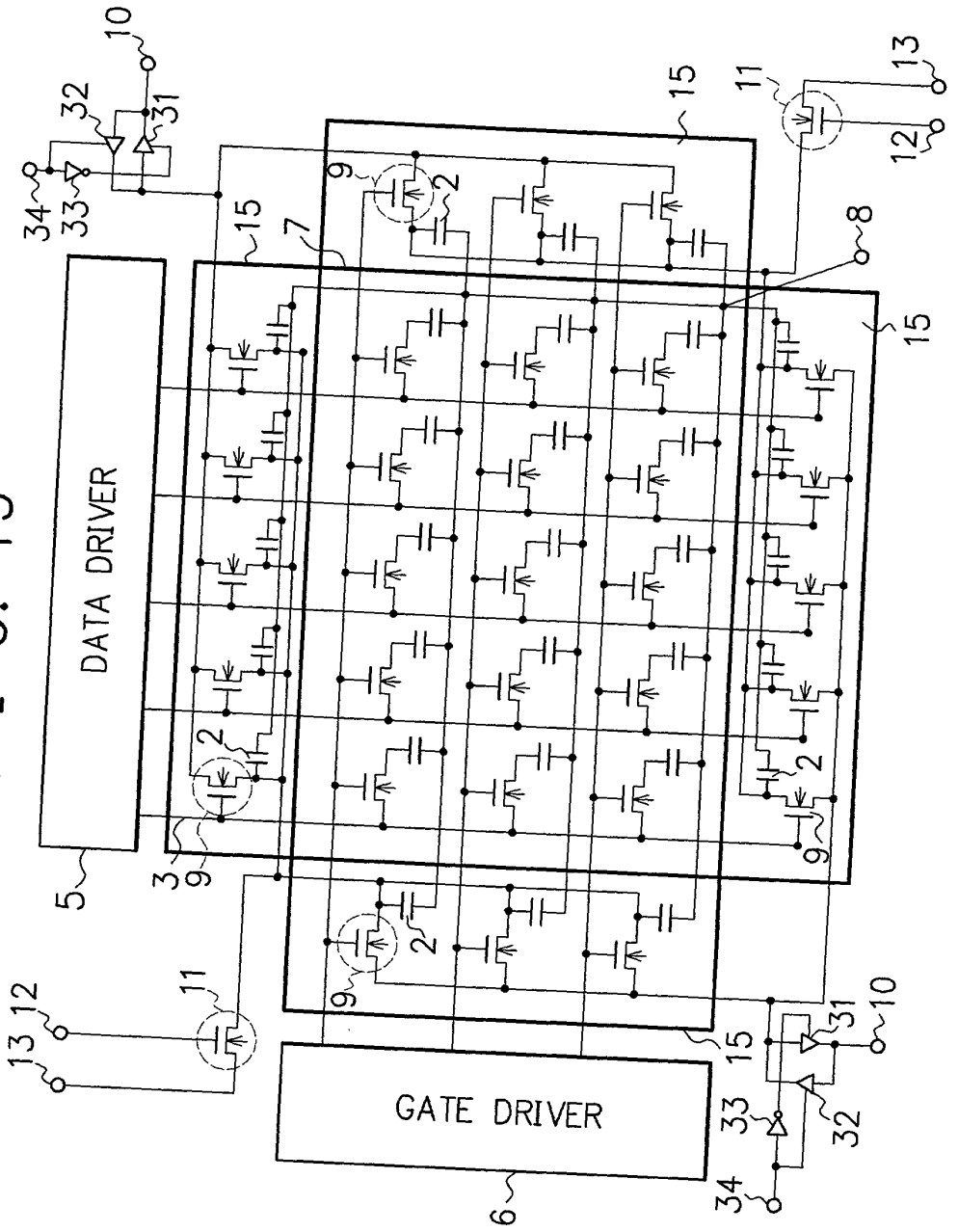


FIG. 20

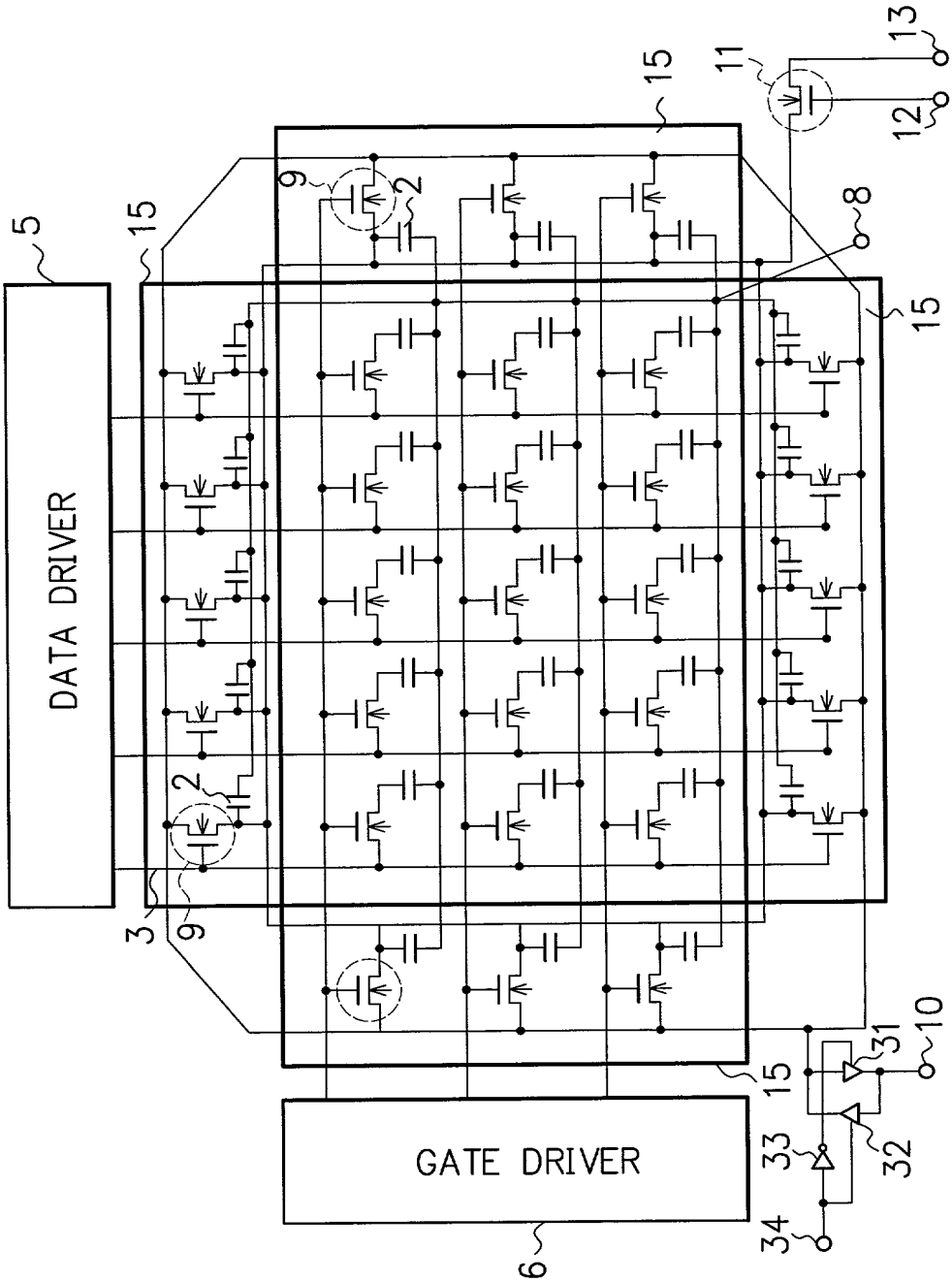


FIG. 21

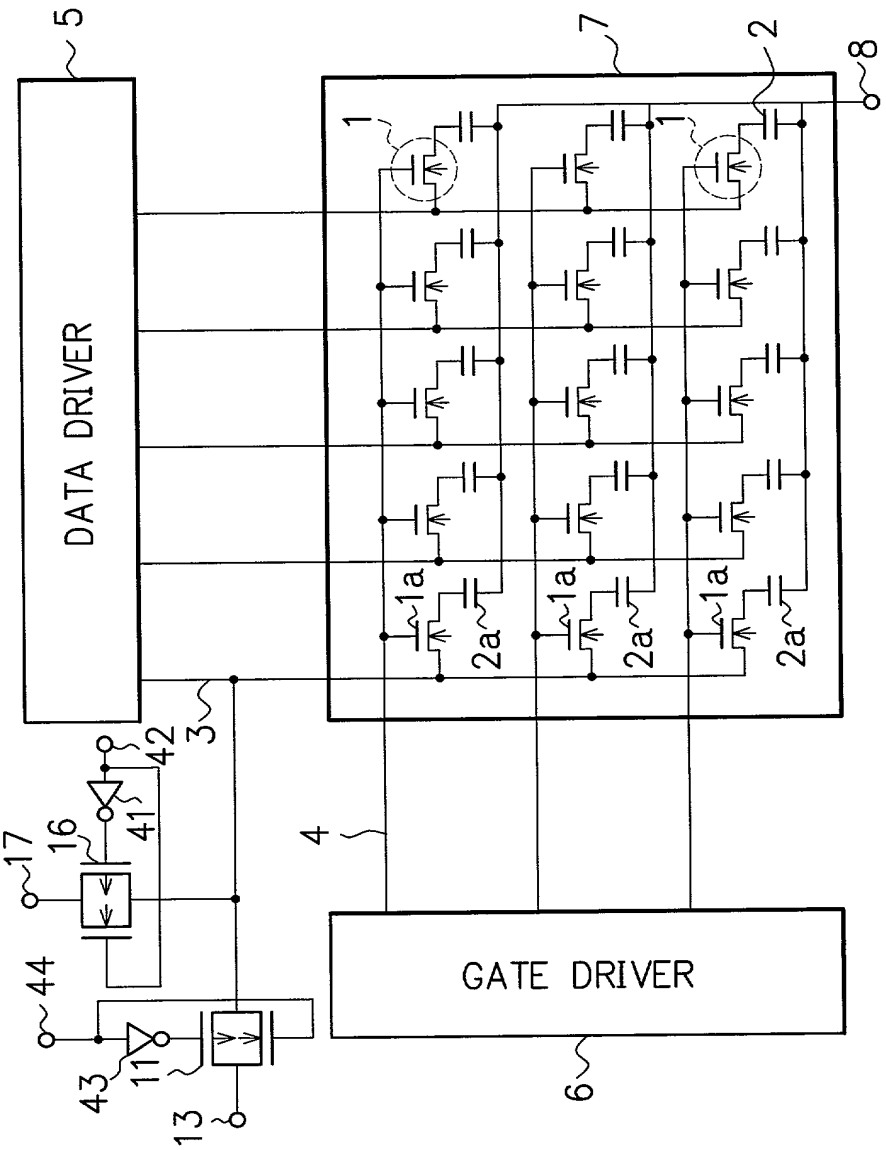


FIG. 22

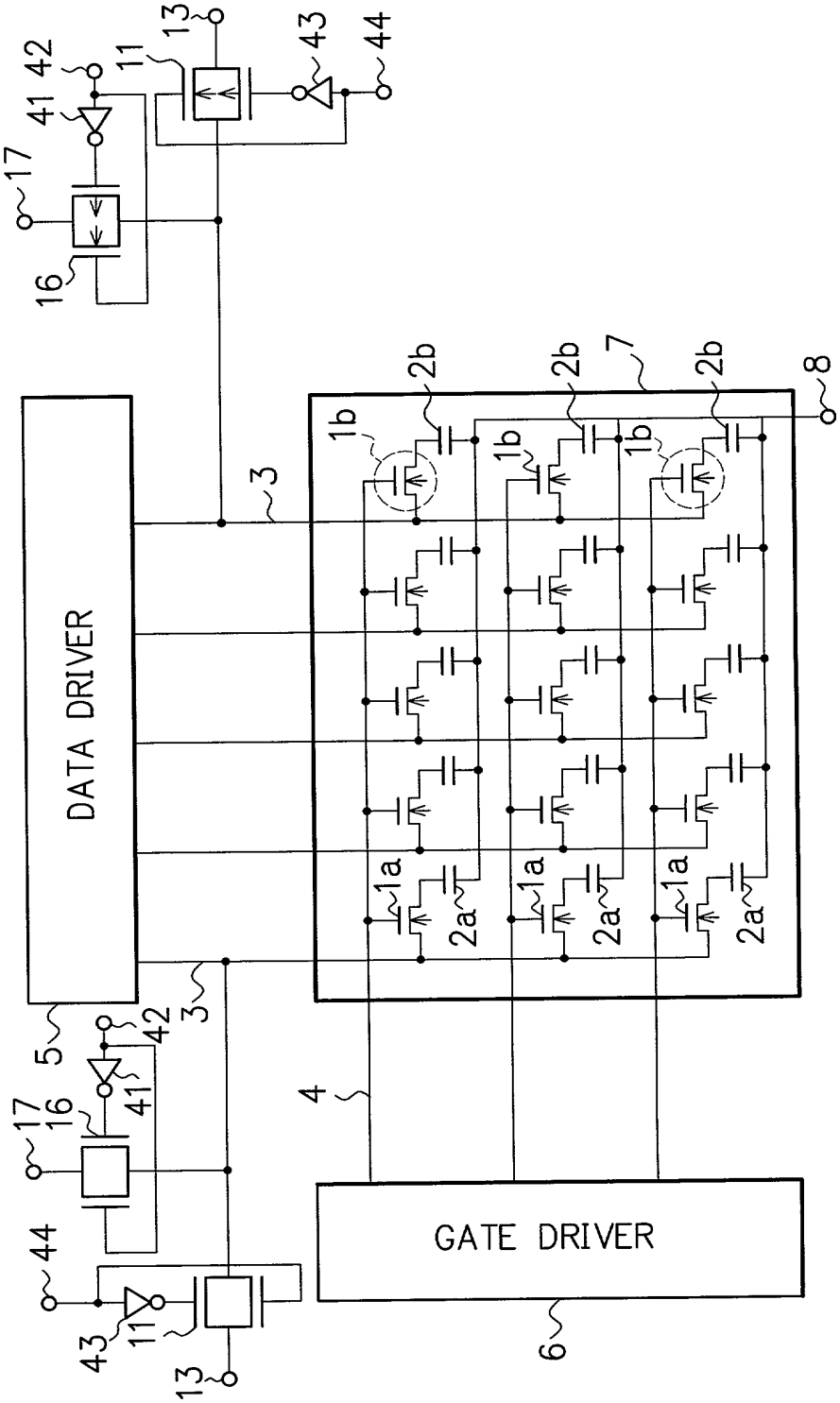

DATA DRIVER
GATE DRIVER
1a
1b
2a
2b
3
4
5
6
7
8
11
13
16
17
41
42
43
44

FIG. 23

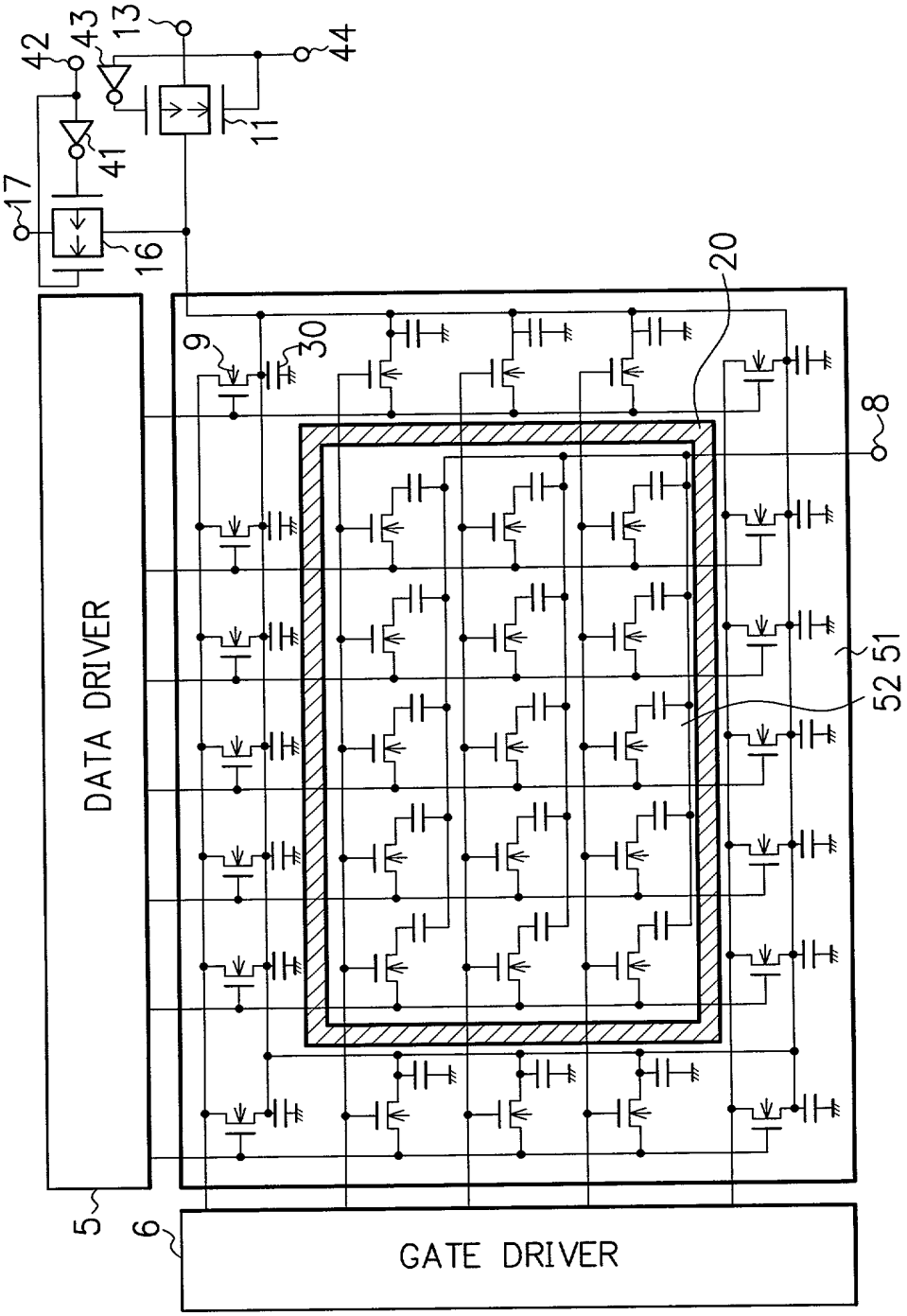
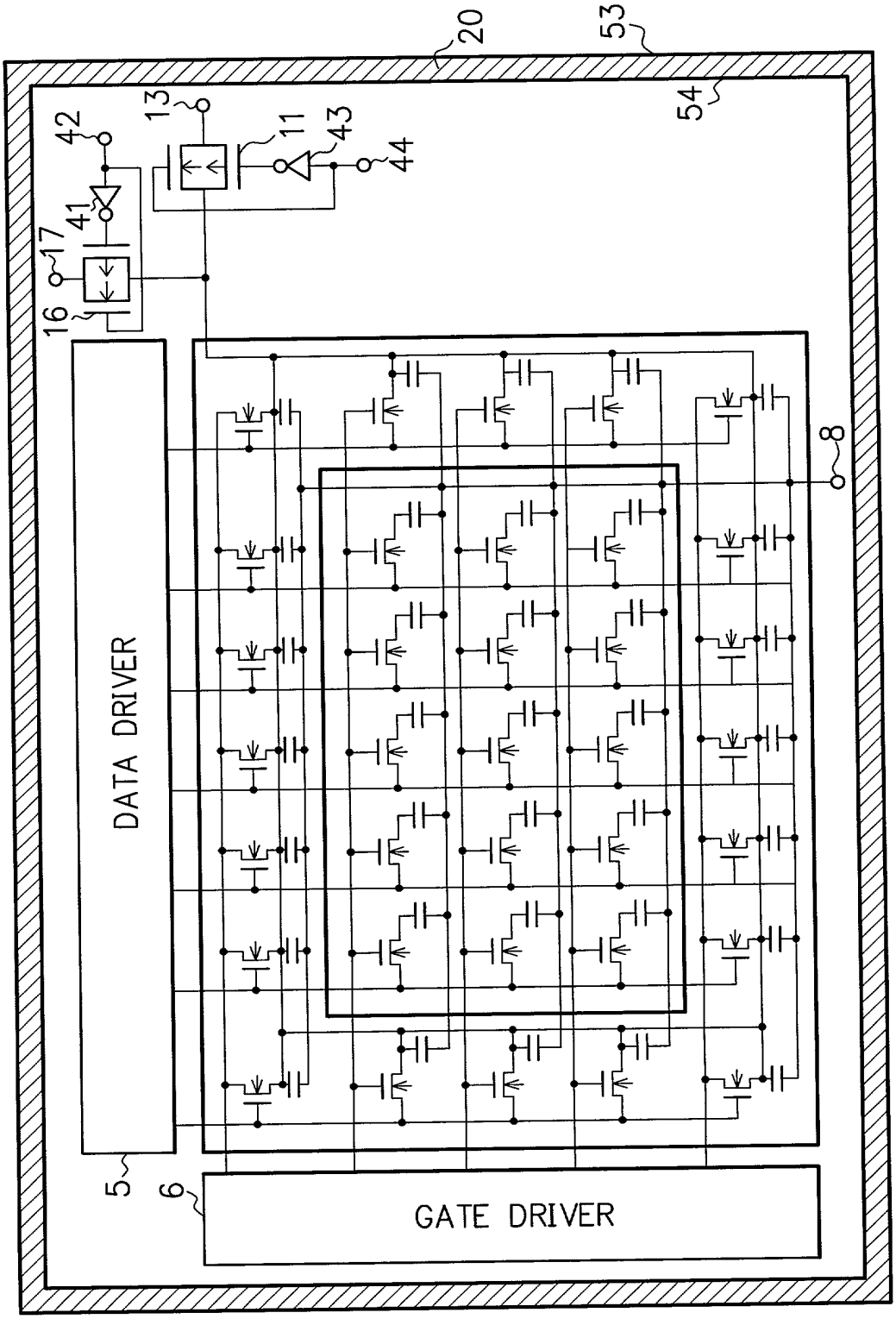


FIG. 24



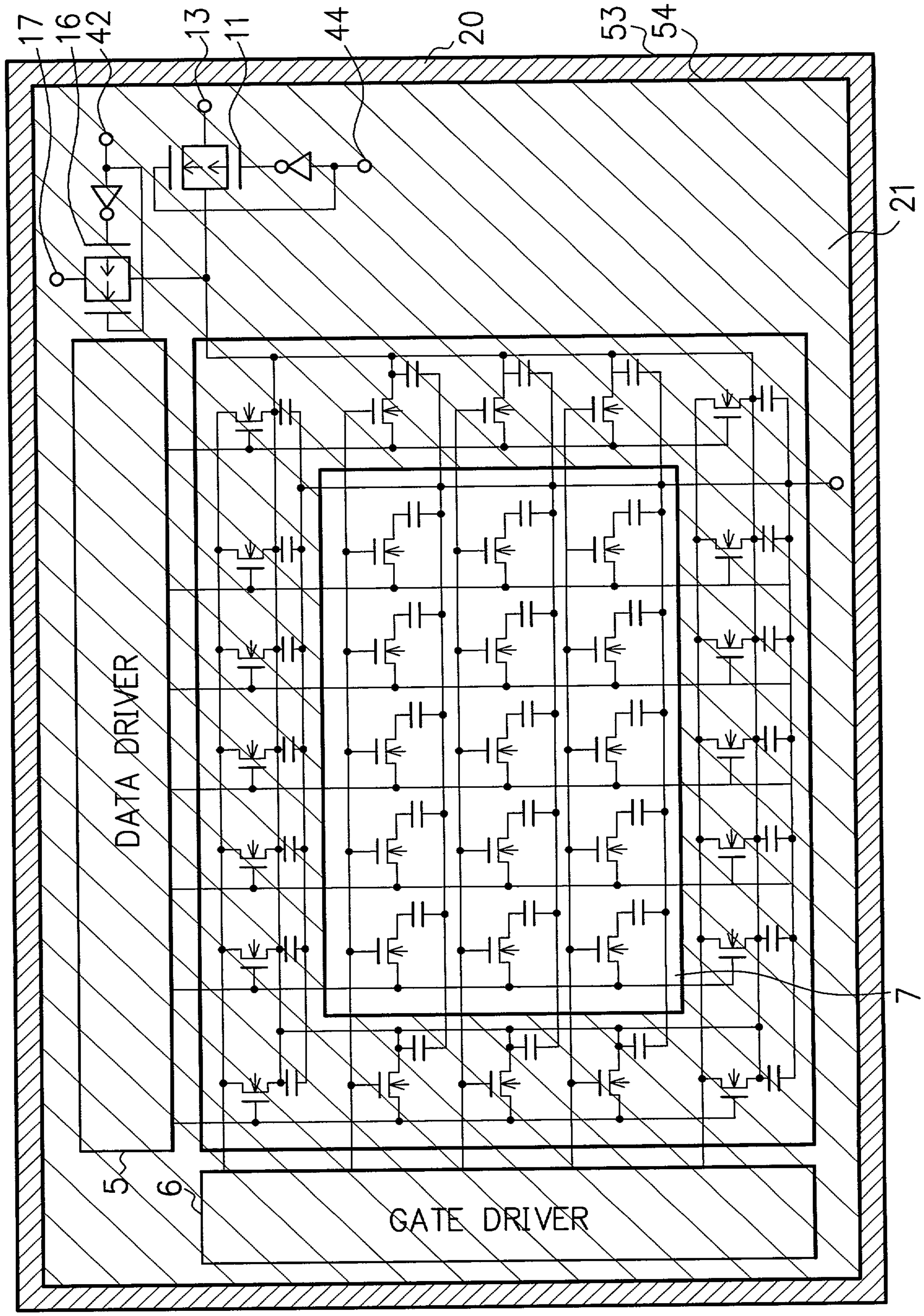
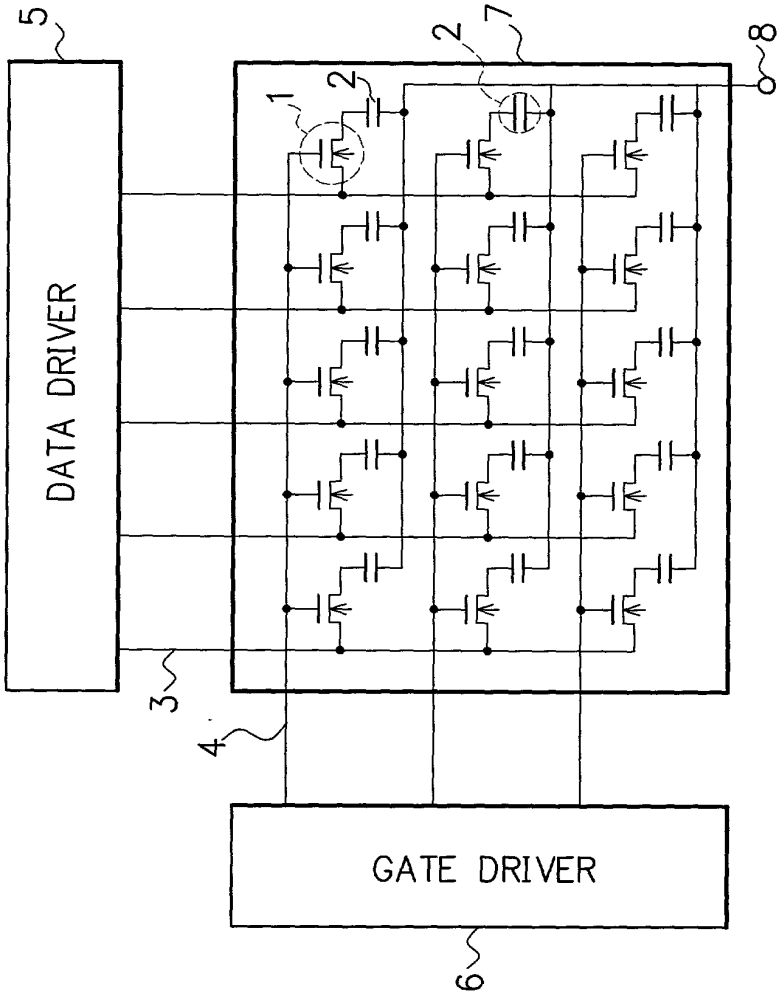


FIG. 25

FIG. 26
PRIOR ART



F I G. 27
PRIOR ART